COLECO INDUSTRIES, Inc.
945 ASYLUM AVE., HARTFORD, CONN. 06105

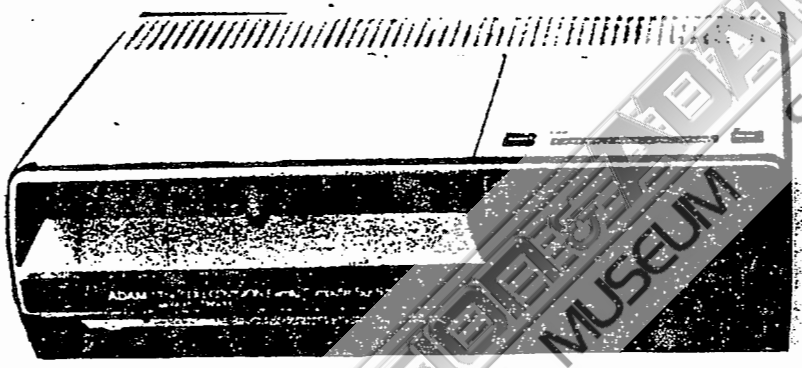
ENGINEERING PERFORMANCE SPECIFICATION # 224

REVISION

ISSUE DATE 10/13/83

TITLE:

DELTA MEMORY MODULE



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EPS # 224

SHEET 2 OF 27

REVISION LISTING

REVISION	PAGE	DATE	SECTION	ECO NO.	DESCRIPTION
Orig Release					

1. PURPOSE

This specification establishes the engineering specification and criteria for the performance of Delta, the host computer module for the Adam home computer system.

2. APPLICABLE DOCUMENTS

#41433	Delta Mechanical Assembly
#41581	Delta Logic Board Assembly
#41843	Delta Logic Schematic
#41580	Delta Game Board Assembly
#41844	Delta Game Schematic
EPS 183	ColecoVision Module
EPS 184	Video Controllers 82-03
EPS 227	Adamnet
EPS 226	Data Drive
	Delta Specification/Bill of Materials
FCC	Part 15, Subpart H
QC	Coleco Home and Office Products Standard
QC108	Sampling Specifications
QC109	Handling and Operating Procedures for MOS Circuits
QC111	Label and Graphic Standards
QC114	P.C. Board Workmanship Standards
NSTA	Preshipment Test Procedures, Project 1A
UL114	For U.S. Systems (Office and Business Equipment)
CSA 22.2	No. 154 for Canadian Systems (Data Processing Equipment)

3. ACCEPTANCE

3.1 AQL (Acceptance Quality Level) of the Delta system when received from the vendor by Coleco Industries, Inc.

1.0 AQL Major (functional defect)

4.0 AQL Minor (nonfunctional defect)

4. ENVIRONMENTAL REQUIREMENTS

At the successful completion of tests for this requirement, the Delta unit shall be tested to performance specification Item 7.

4.1 Operating Temperature and Humidity Range: + 10°C (50°F) to 40°C (104°F) at 10% to 80% RH (non-condensing)

4.2 Storage Temperature and Humidity Range: -10°C (14°F) to +60°C (140°F) at 0% to 90% RH

4.3 Thermal Cycle:(unpowered) Shall withstand 10 thermal shock cycles. Each cycle includes one hour at each operating temperature extreme and one hour of stabilization at room temperature between each extreme; i.e, Hot, Ambient, Cold, Ambient (each temperature for one hour).

4.4 Electrostatic Discharge Test: At all switches, housing openings, parting line, any metal surfaces shall withstand 25 KV discharge from a 200 pf capacitor with 10K ohms limiting resistor.

4.5 Vibration: Packaged unit shall comply with NSTA Preshipment Test Standards, Project 1A

4.6 Drop Test: Packaged unit shall comply with NSTA Preshipment Test Standards, Project 1A

4.7 Radio Frequency Interval: Shall comply with FCC Class B, Subpart H, Part 15

5. APPLICABLE STANDARDS

This section deleted - Refer to Section 2.

6. LIFE

Note: Life requirements provided below are superseded by those provided on the latest revision of the referenced print (part #).

6.1 1000 hours minimum, the Delta unit shall be tested as follows: Ambient 25°C at 50% ± 10% RH connected to Printer Power Supply (EPS 223) and the 62500-baud communications interface (Adamnet) (EPS 227).

6.2 Cartridge Edge Connector (30-pin) #75451: minimum 5,000 insertions @ 400-600 insertions/hour with contact resistance 0.5 ohms maximum. Contact resistance shall be determined with a virgin cartridge PCB before and after insertion test. Insertion test cartridge PCB must be less than 0.5 ohms contact resistance measured on a virgin cartridge connector.

6.3 Cartridge Door Assembly #41497: minimum 5000 openings tested to 90° of travel.

6.4 Reset Switch (Game) #72501: minimum 10,000 operations (15/18 cycles per minute) with contact resistance not to exceed .03 ohms. Switch to withstand 500V for 1 minute.

6.5 Reset Switch Assembly (Computer) #41572: Minimum 10,000 operations (15/18 cycles per minute) with contact resistance not to exceed .03 ohms. Switch to withstand 500V for 1 minute.

6.6 R.F. Switch Box #74608: 10,000 operations minimum. Phono jack: 350 insertions/withdrawals minimum (with coax).

6.7 Modular Connector, 6-pin female #42202 (from keyboard), minimum 1000 insertions of mating cord #41027; maximum retention force = 17 pounds; maximum contact resistance = 0.2 ohms.

6.8 Modular Connector, 6-pin female #41020 (for future expansion), minimum 1000 insertions of mating cord #41027; maximum retention force = 17 pounds; maximum contact resistance = 0.2 ohms.

6.9 Expansion Port Door #41423: 1000 openings/closings minimum.

6.10 Expansion Port Edge Connector (60-pin) #41534: minimum 1000 insertions/withdrawals. Maximum insertion force = 25 pounds and minimum withdrawal force = 5 pounds. Maximum contact resistance = 0.1 ohms. Shall be tested with a virgin female edge connector only. Female test connector must be less than 0.1 ohms contact resistance and within force specification measured on a virgin male connector.

6.11 Power Connector "D" type (male) #75450: 200 insertions/withdrawals minimum with mating connector # 41277 (from printer). Contact resistance .005 ohms maximum. Maximum insertion force: 15 pounds and minimum withdrawal force: 5 pounds. Disregard 1st insertion withdrawal.

6.12 Controller Connector "D" Type (male) #75450: 200 insertions/ withdrawals (with cable). Maximum insertion force: 15 pounds.

Minimum withdrawal force: 5 pounds. Maximum contact resistance: 0.5 ohms. Insertion/withdrawal force, contact resistance shall be determined with a virgin "D" connector. Insertion test "D" connector must be less than 0.5 ohms contact resistance and within force specification measured on a virgin male "D" connector.

6.13 R.F. Cable #78174 shall be 75 ohms and equipped with RCA jack; both ends to fit socket (coax phone jack socket #73457) 350 insertions/withdrawals 0.03 ohms contact resistance maximum.

6.14 Coax Phone Jack Socket #73457 (2): 500 insertions/withdrawals minimum (with coax) 0.03 ohms contact resistance maximum.

6.15 Circular Connector (7-pin) #41579: 500 insertions/withdrawals minimum (with mating cable #41647) 0.03 ohms contact resistance

6.16 Channel Select Switch (3-4) #74934 minimum 1000 operations with contact resistance not to exceed 0.03 ohms

6.17 Logic Board Assembly Connector Life:

Each connector to be tested with proper mating connector for 1000 cycles at less than 1 cycle per second. Contact resistance is to be less than 50 milliohms throughout the entire test. Maximum insertion force is to be 12 pounds and minimum withdrawal force is to be 5 pounds, unless otherwise stated. These connectors include:

- o 41582 - PCB interconnect (Delta Logic and Game PCB)
- o 41279 - 44-pin connector (Expansion slot)
- o 75451 - 30-pin connectors (Expansion slot and I.C)
- o 41530 - 9-pin friction lockwafer (data drive)
- o 41631 - 8-pin friction lockwafer (data drive)

7. PERFORMANCE SPECIFICATIONS

7.1 Engineering Test Conditions

7.1.1 A power supply as specified in 7.2 is required for providing power to the Delta unit for performing any test in the specification.

7.1.2 Ambient environment shall be 25°C at 50% ± 10% RH unless otherwise noted.

7.1.3 The Delta unit shall be stabilized to ambient condition for one hour before testing.

7.1.4 The test shall be performed using a color TV set, the printer, keyboard, an Adam system test cartridge, and a Buck Rogers tape.

7.2 Power Supply Requirement

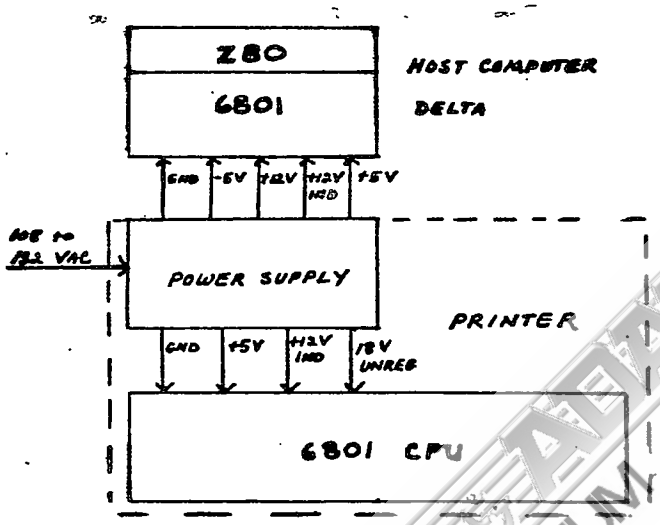
Power is provided by the Printer Power Supply (EPS 223)

The nominals input to the Gamma PCB in 5 parallel lines are:

GND		
+5VDC	(+6%) (-3%)	
-5VDC	(-7%) (+5%)	(See Figure 1.)
+12VDC Inductive	(±5%)	
+12VDC Logic	(±5%)	

Ripple: All DC Voltages shall have no more than 10mV pp.

Figure 1. Delta Power Supply



7.3 Communication Interface (Adamnet, EPS 227)

The Delta unit shall be connected to the printer/keyboard/cassette via a 62500-baud, half duplex, serial communications link (Adamnet).

7.4 RF Requirements

7.4.1 Two selectable channels, 3 and 4 shall be available, video carrier frequency requirement to be:

- Channel 3 - 61.25 ± 0.25 MHz
- Channel 4 - 67.25 ± 0.5 MHz

7.4.2 Peak amplitude level between 1200-3000 uV into 75 ohm.

7.4.3 Sound carrier frequency to be ±4.5 MHz ±15K Hz away from the video carrier frequency.

7.4.4 Sound carrier amplitude level shall be maximum 77 uv (-69 dbm) and shall fall no more than -25db below the video when terminated and matched with a 50 ohms load.

7.4.5 Color subcarrier frequency shall be ±3.579545 MHz ± 125 Hz at each side of video carrier.

7.4.6 At RF output terminal #73457, the maximum voltage of any emission appearing on frequencies removed by more than 4.25 MHz below or 7.75 MHz above the video carrier frequency shall not exceed -69dbm(77uv) when terminated and matched with a 50 ohms load.

7.4.7 Radiation interference limits, line-conducted interference limits and transfer switch #74934 shall meet FCC Part 15, sub-part H specification on TV interface devices.

7.4.8 Output return loss when terminated with a 75 ohms resistance load shall not exceed 16 db.

7.4.9 Index of video carrier modulation shall be 60 to 90%. Output signal to noise level shall be higher than 57 db.

7.5 Clock Frequency

7.5.1 Game PCB Main Clock

Clock frequency shall be 3.579545 MHz ± 125 Hz at U8 pin 9

Rise and fall time to be maximum 15 ns between 0.8 to 4.4V

Logic high to be minimum 120 ns from 4.4 to 5.3 VDC.

Logic low to be minimum 120 ns from -0.3 to 0.8 VDC.

7.5.2 Video Chip Clock

Clock frequency shall be 10.738635 MHz ± 375 Hz at U9 pin 40

Rise or fall time to be 15 ns max. between 0.8 and 2.4V, and total combined rise and fall time to be 20 ns max.

Logic high to be above 2.4V and min. 40 ns at 2.4V level.

Logic low to be below 0.8V and min. 33 ns at 0.8V level.

7.5.3 7.1 MHZ Clock

Clock frequency shall be 7.159090 MHz ± 250Hz at U8 pin 11

Clock duty cycle shall not be more than 70%.

Logic high to be above 2.0V

Logic low to be below 0.8V.

7.5.4 Computer Logic PCB Clock

This clock is generated by an oscillator circuit which is internal to the 6801 microprocessor and requires only an external crystal. To assure proper oscillator function, 1.0 MHz ± 500 Hz shall be measured on pin 40 of the 6801 CPU.

7.6 RF Frequency shift shall be within the following limits from the original calibrated setting:

7.6.1. Operating temperature range	± 75 KHz
7.6.2 Operating humidity range	± 75 KHz
7.6.3 Vibration Test	± 75 KHz
7.6.4 Drop Test	± 75 KHz
7.6.5 Line voltage range	± 5 KHz
7.6.6 Thermal cycling test	± 75 KHz
7.6.7 Short-term frequency drifts	± 350 KHz
7.6.8 Long-term frequency drifts	± 350 KHz
7.6.9 Combination of 7.6.1 to 7.6.7	± 350 KHz

7.7 Composite Video Signal

The composite video signal shall meet American NTSC System standards. Details of the specification requirements for Color and Timing are provided in ColecoVision EPS 183. (Section 7.8)

7.8 Expansion Port and Connectors

Details for Expansion Port J2, J1, and Hand Controller Connectors J5 and J6 are provided in ColecoVision EPS 183. (Section 7.9)

7.9 System Test Specifications

The system test shall be run in two phases. In the Phase I test, an Adam test cartridge is used. This test is described in detail in Section 7.9.1. In the Phase II test, a Buck Rogers tape is used; this test is described in Section 7.9.2.

7.9.1 Phase I Test

The Adam System Test is a go/no go test. To reset, the operator can hit Game Reset. The test includes the following:

1) Hand controller test, super controller included for spinner test
2) Audio and video test
3) Printer test - sends 16 characters to the Printer
4) Data drive test - writes, reads, and verifies a sector on both tracks of tape drive zero
5) RAM Memory Test - performs a memory test on the main (64 K) memory
6) Checksum on ROM - calculates the checksum of the Delta Game Board operating system ROM and the four ROM's on the Computer Logic Board

7) Keyboard Test - inputs and echoes characters from the keyboard

If any part of the test routine becomes erratic, the test will be considered as failed. In any segment of the test, one error readout in three tries is classified as a soft error. Any two errors in three tries is classified as a hard error.

- Power-up - Test cartridge not inserted

  When the main power switch is turned on and the cartridge reset switch is activated, Figure 2 will appear on screen, pattern and color as noted.

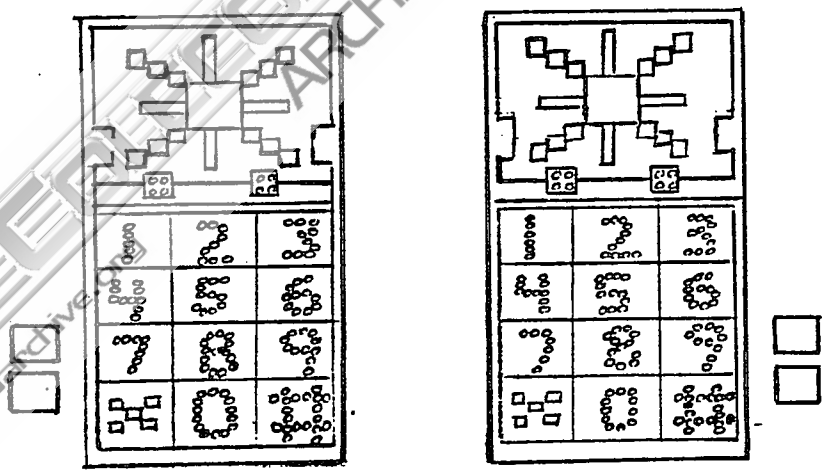
Figure 2. Power-up W/O Cartridge

- Power-up - Test cartridge inserted. Upon turn-on of the main power switch, with the cartridge reset switch activated, the test sequence begins:

1) Hand Controller and Super Controller Test

Pictures of the hand controller will appear on the screen as shown in Figure 3. The two green squares on the outside of each of the controllers represent the two lower buttons on the super controller. This test is interactive. When the operator presses the lower two buttons on the super controller, the green squares will disappear; when the operator operates the spinner, the two squares on the screen controllers flash; one on the left, one on the right. Operation of the joystick makes the bars around the blue axis disappear one at a time. Pressing the keys on the numeric pad of the controller makes the numbers on the screen controller disappear. Each key on the pad must be depressed before starting the Audio and Video Test.

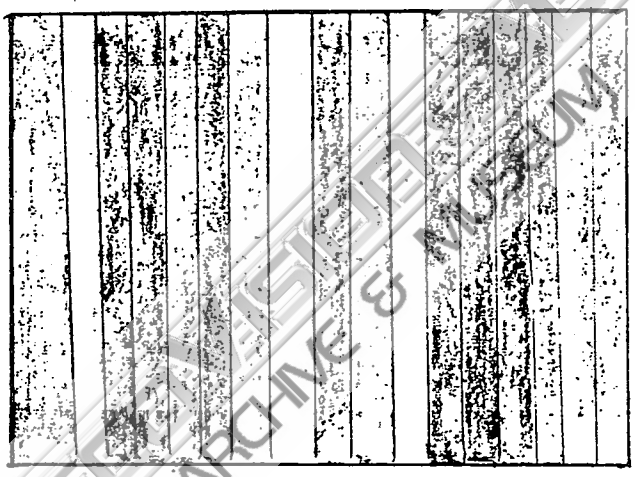
Figure 3 - Hand Controller Test



2) Audio and Video Test

Immediately following the controller test, vertical bars (as shown in Figure 4) appear on the screen for about five seconds. There is a sharp distinction between each of the bars which appear in a clear, snowless picture. Colors should conform closely to the NTSC color bar pattern. Anything other than solid bars of color indicates a possible problem in the video RAM and/or chip.

Figure 4 - Audio and Video Test



At the same time that the video display appears on screen, three musical tones and one noise register sound. These sounds should be clear and without any noticeable background noise.

To abort this portion of the test, the operator can hit any key on the hand controller.

3) Printer Test

Also, at the time of the video display, 16 functions/characters are being sent to the system printer. These functions/characters represent various functions and combinations of upper case, lower case, and numeric characters on the daisy print wheel. See Figure 5.

(characters)	(functions)
test AB 12 &	Carriage Return and Line Feeds

Figure 5 - Printer Test

4) Tape Drive Test

The print test is followed by the tape drive being activated. The data drive assembly rewinds the tape in Drive 0. A sector on each tape (Track 1 and Track 2) is written to, read, and verified on Tape Drive 0. When this portion of the test is completed, a message will appear on the screen: Tape Drive 0 is OK or Tape Drive 0 is Bad.

5) RAM Memory Test on Main (64K) Memory

Figure 6 will appear on the screen indicating test on the 64K RAM is in process. Successful completion of this test will be indicated by an OK readout of both the upper and lower segments, as shown in the figure.

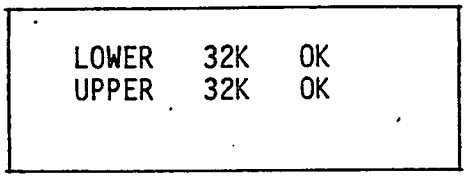


Figure 6 - Main Memory Test

6) ROM Test of Checksum

Figure 7 will appear on the screen indicating tests on the Game Board operating system (CV OS) ROM and the four ROM's on the Computer Logic Board are in process. The operator can verify the checksum with its accepted value, as shown in the figure.

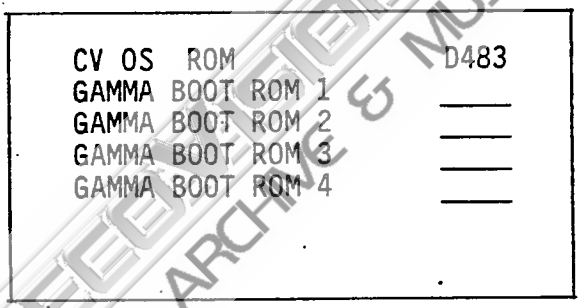


Figure 7 - ROM Test

7) Keyboard Test

This test is interactive. The operator hits various keys on the keyboard which, as a result, appear on the screen. The operator then can verify that those characters that appear on the screen are the same as those keys that were depressed.

7.9.2 Phase II System Test

After the successful completion of the Phase I test, a bootup will be performed on the system. This test will be performed using the Buck Rogers tape and occurs in the following sequence:

1) The power is turned off
2) The Buck Rogers tape is inserted
3) The power is turned on
4) A check is made on the time required to boot the system up.

Bootup from start to finish should be within a timeframe of 2 1/2 to 3 minutes; worst case being 3 minutes. If the first attempt fails, a second cassette should be inserted. A second failure will be considered a hard fail.

8. PRODUCT DESCRIPTION

8.1 General

The Delta unit is the memory console for the Adam home computer system: it combines the ColecoVision (Game) PCB and subsystems with the Computer Logic PCB in one module. The Data Drive Assembly (EPS 226) and Game Controllers are included in the Delta System as well. The Delta unit combined with the Keyboard unit (EPS 220) and the Printer (EPS 221) make up the Adam home computer system.. See Figure 8.

Figure 8. Adam System Functional Block Diagram

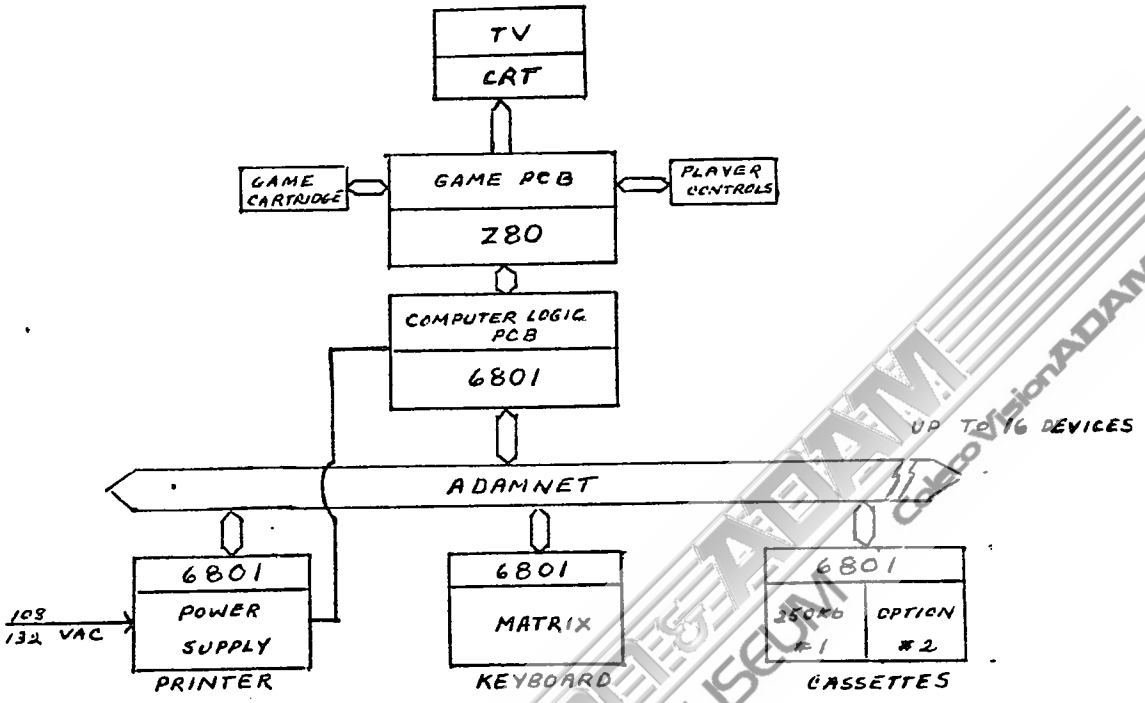


Figure 9 shows the various input/output leads and connections to the Delta Console.

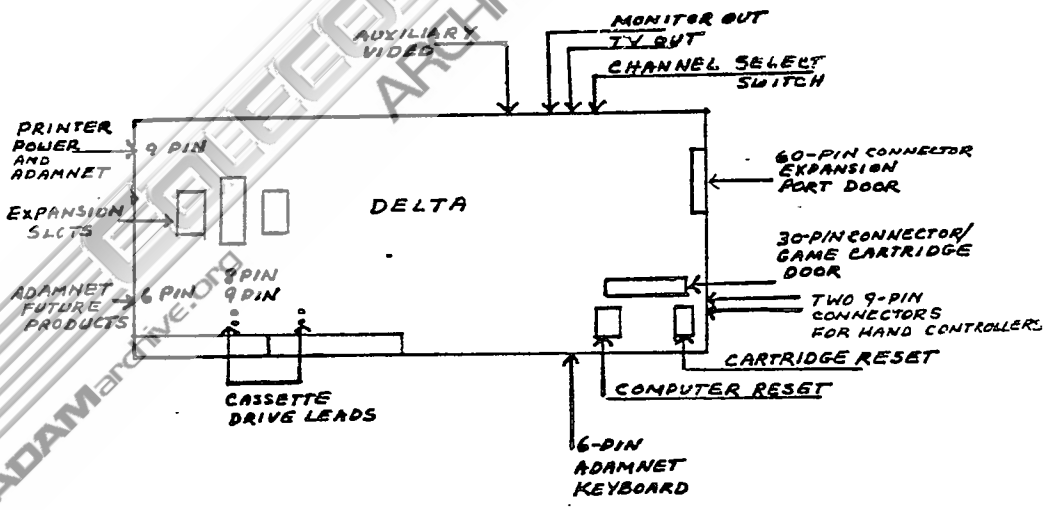


Figure 9. Delta Connections

The Delta console has two door openings: one for the game cartridge and one for the expansion module. A spring-return door protects the 30-pin female edge connector and ensures the proper insertion of the game cartridge; a pivoting door protects the 60-pin male edge connector used to connect expansion modules. Two reset switches are provided to reset the console to the start-up mode: one for cartridge reset, one for computer reset.

Power is furnished to the Delta console by the Printer Power Supply (EPS 223) via a 9-pin male connector. Two male 9-pin connectors are provided for the controllers and two 6-pin communication links (Adamnet EPS 227) connect the keyboard and future products to the console. The power supply is furnished to the keyboard through this link as well.

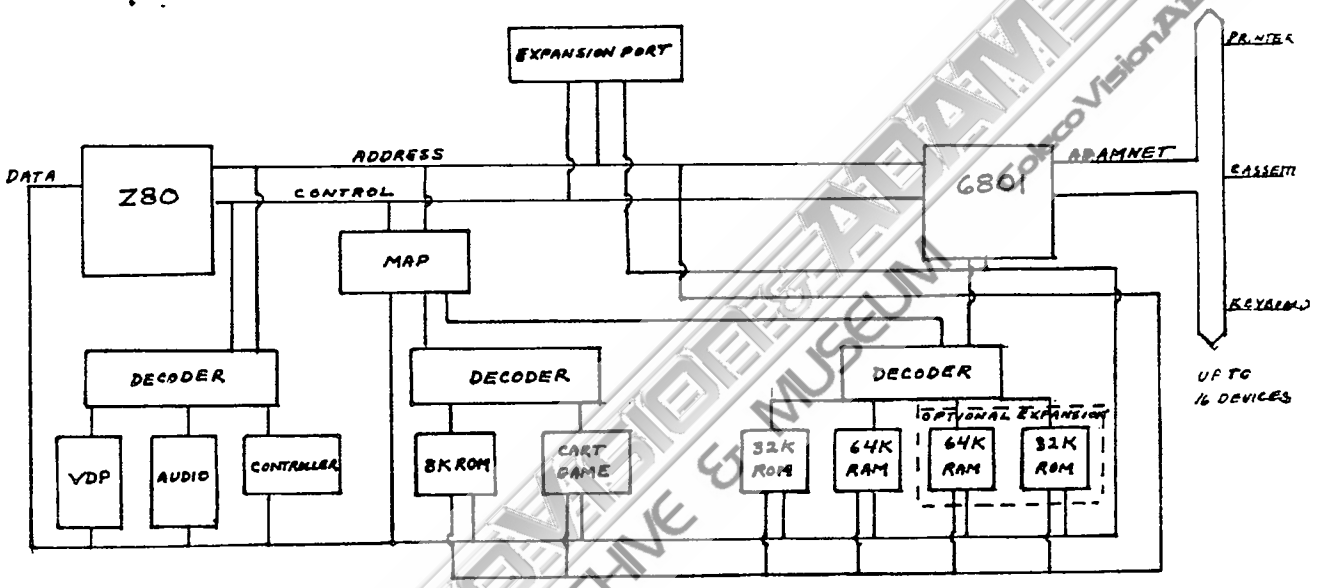
The RF channel select switch is located on the back of the console where three cable jack connections are also provided. These connections include TV Out, Monitor Out, and Auxiliary Video. The system ON/OFF switch is located on the back of the Printer.

8.2 Technical System

Two PCB's, fully shielded to FCC Part 15 requirements, make up the Delta system: the Game PCB and the Computer Logic PCB. The Game PCB consists of five major systems: namely, the Z80 CPU, Video Display Generator, Audio Generator, RF Section, and the Game Controller Section. The Game system clock operates at 3.58 MHz. The Computer logic PCB consists of two major systems: the 6801 CPU and the Adamnet Communications

link (EPS 227). An on-board clock and crystal oscillator provide the 4.0 MHz clock for the Computer logic PCB. Expansion slots are included for an optional ROM card (32K ROM), a real time clock, and an additional 64K RAM. A functional block diagram of the Delta system is shown in Figure 10.

Figure 10. Delta Functional Block Diagram



8.2.1 Z80 CPU System

The Z80 CPU system operates in one of two modes, either the Game mode or the Computer mode. The mode of operation is determined by the memory map shown in Figure 11.

Figure 11. Memory Map

LOWER MEMORY	0000H	CV OS 8K ROM	COMPUTER ROM 32K	DRAM 32K	OPTIONAL ADD-ON DRAM 32K
	2000H 7FFFH	DRAM 24K			
UPPER MEMORY	8000H FFFFH	CARTRIDGE 32K ROM	DRAM 32K	OPTIONAL ADD-ON ROM 32K	OPTIONAL ADD-ON DRAM 32K

The Z80 CPU system is capable of configuring the memory map into any combination of lower and upper memory and switching between them. A M1 wait-request hardware has been included in the system enabling the Z80 to automatically introduce one clock period to the fetch cycle. As a result, the memories timing requirements are as follows:

ColecoVision (Game) Operating System (CV OS)

- Access time from chip select to data output valid....150 ns max.
- Access time from address valid to data output valid...450 ns max.

Computer ROM

- Access time from chip select to data output valid....150 ns max.
- Access time from address valid to data output valid...450 ns max.

DRAM

- Access time from Row Address strobe....250 ns max.
- Access time from Column Address strobe...165 ns max.

The Z80's available connections, in addition to affording direct access by the Game system, provide access to the Computer logic PCB (CPU 6801). The two systems combine to make up Delta, the host computer for the Adam Home Computer System.

8.2.2 Video Display Generator

The video display is generated by the TI 9928 and directly output video R-Y, B-Y, Y signals to the RF section. The 9928 uses a table-driven architecture which allows the programmer to control every pixel in the visual display area. In addition, it allows the programmer to define and control 32 objects or "sprites" which may be placed anywhere on the display and moved around at will. The VDP chip is addressable in "data mode" (used whenever VRAM is being written or read) and "register mode" (used when control information is being written to and read from one of the chip's internal registers). The addresses of these ports in the CPU I/O address space are as follows:

- Data Port .... OBEH
- Register Port .... OBFH

The VDP is driven by 10.7 MHz clock pulse as specified on Item #7.52 which is obtained from the third multiple, high Q tuned tank circuit on the 3.58 MHz system clock. As this chip is sensitive to noise, a LC filter circuit has been added to its Vcc supply line to eliminate the audio interference on video. The VDP and the VRAM's are the principal heat generation sources. Therefore, necessary hardwares, heat sinks, and physical layout, etc., were considered and applied to lower temperatures to within limits. Since the VDP has a 10.7 MHz clock, the access time

for the VRAM is 200 ns parts maximum.

8.2.3 Audio Generator

The system uses a TI76489 sound generator controller to produce sounds. The chip contains three programmable tone generators, a programmable white-noise generator, and programmable attenuation for each of these channels. The chip is addressed through a single port which may be called a sound port. Wait-request hardware has been included in the system because the sound chip is a slow peripheral requiring data lines to be stable for a relatively long time while writing to it. Location of the sound port in the CPU's I/O address space is OFFH.

8.2.4 RF System

This section utilizes the NS chip 1889 to interface audio, color difference and luminance signals to the antenna terminals of a TV receiver. It consists of two VHF channels, 3 or 4, selectable by a slide switch with determined LC tank circuits. The Chroma subcarrier oscillation is obtained from the 3.58 MHz system clock to ensure the accuracy and stability. The sound oscillator's frequency modulator is achieved by using a 4.5 MHz tank circuit and deviating the center frequency via a varactor diode. Due to the incompatible signal level between the VDP 9928 and the 1889, a DC restoration circuit has been added to ensure the DC level of the video signal.

8.2.5 Game Controllers

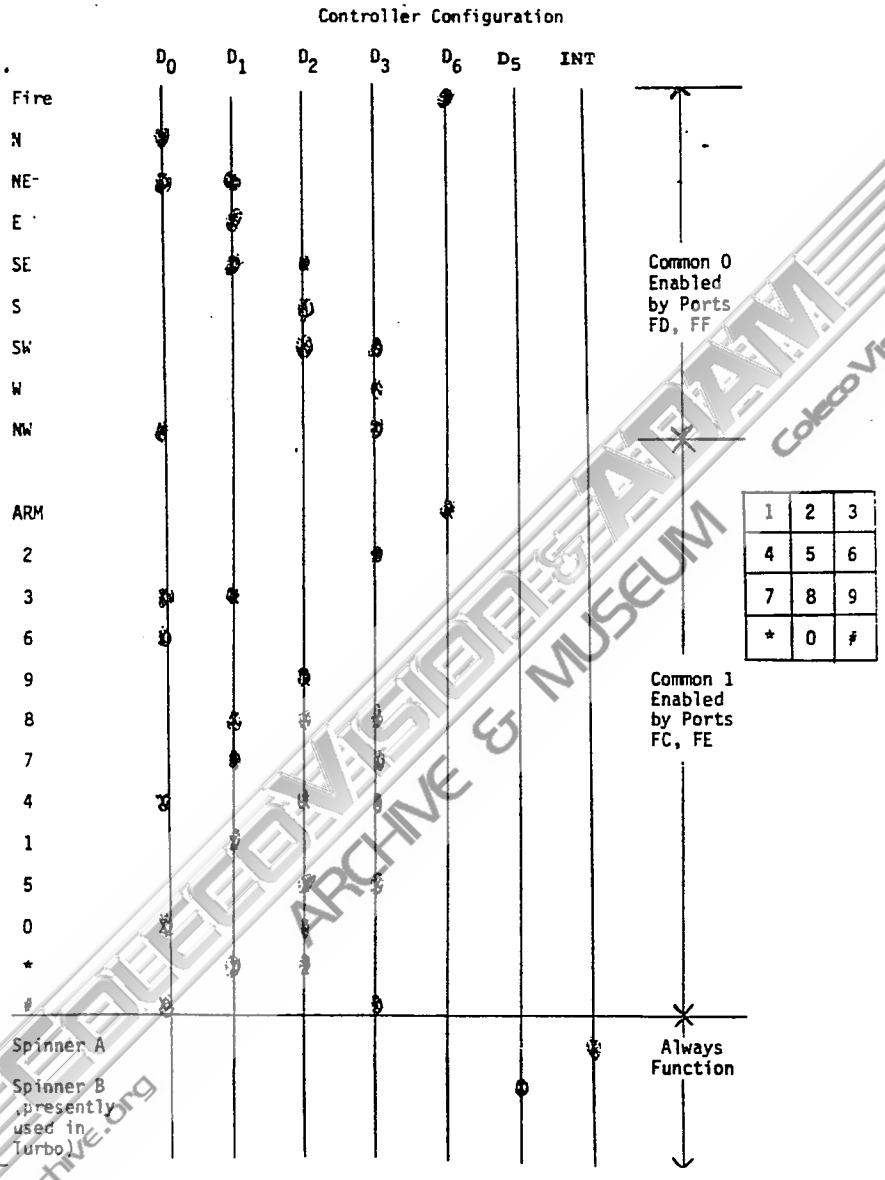
Two game controllers are provided with the Delta System . They are identical to those provided with the ColecoVision Module. (See EPS 183.)

On each controller are: an 8-position joystick, two reaction keys called Fire and Arm, and a 12-key numeric keypad. Each controller is accessed by the system through its own own port. The address of these ports in the system I/O address are as follows:

- Controller #1 OFCH
- Controller #2 OFFH

For each controller, 18 switches are read on a single 8-bit port. Therefore, once a port has been read, some decoding is required to determine which switches have been depressed. The layout and the encoding of the various controller functions is shown in Figure 12. There are two spinner switches which are not wired in the controller and will be used in games such as Turbo. In order to assure that the spinner switch closures are always processed as soon as they happen, they are connected to the CPU maskable interrupt, and the cartridge software determines which switch will cause the interrupt.

Figure 12. Controller Encoding and Functions



8.2.7 Adamnet (For Details, see EPS 227)

As shown in Figure 8, Adamnet is the main bus or network that connects all devices to the Adam home computer system. Adamnet is a 62500-baud, half duplex, serial communications link over which all information is passed.

8.2.8 Data Drive Assembly (For details, see EPS 226)

The Data Drive assembly provides for two cassettes: one is included with the system, the other is optional. Each cassette adds 250K byte of external memory to the Adam home computer system. The Data Drive assembly is a computer-controlled, digital cassette drive system. Two printed circuit boards are included: the servo board that controls the direction and speed of the cassette by providing motion control to the two motors, and the R/W PC board that facilitates storage of data onto the tape and readback of data from the tape. The 6801 CPU for the Data Drive assembly is located on the computer logic board of the Delta Module.

8.2.9 Internal Expansion Slots A, B & C are provided for the following options:

A. Additional 64K byte RAM

B. Additional 32K byte ROM

C. Real Time Clock